JUSTIN COPPOLA

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EDUCATION

University of Florida **Gainesville, FL**
Master of Science in Electrical and Computer Engineering | GPA: 3.79 *Expected: May 2027*

- **IBM ALAP Recipient**: Selected for IBM-sponsored graduate tuition assistance
- **Relative Coursework**: Reconfigurable Computing 2, Engineering Leadership, Future of Semiconductor Tech.

University of Florida **Gainesville, FL**
Bachelor of Science in Electrical Engineering *May 2025*

- **Awards/Honors:** 2022 Dean's List, Order of the Eastern Star scholarship recipient, Mensa Society
- **Leadership:** Theta Tau Professional Engineering Fraternity – Leadership Chairman

TECHNICAL SKILLS

Design & Test: ASIC Design, Design for Test (DFT), RTL Design, Design Verification, Scan Insertion, MBIST, ATPG
EDA Tools: Synopsys DFT Flow, Synopsys Testmax & Design Compiler, Verdi, Cadence, Vivado, ModelSim, Quartus
Programming & Scripting: SystemVerilog, Verilog, VHDL, Python, TCL, Bash, C, C++, MATLAB, HTML, JavaScript
Development Tools: Git, Jenkins, Linux (CLI), CI/CD, REST APIs

PROFESSIONAL EXPERIENCE

IBM **Rochester, MN**
Design for Test Engineer – Quantum Control ASICs *August 2025 – Present*

- Implement Design-for-Test (DFT) methodology for room-temperature quantum ASICs using the Synopsys DFT flow, supporting macro-level and chip-level integration from initial bring-up through implementation
- Designed and developed an internal DFT Hub that automatically parses Synopsys Testmax, Design Compiler, and ATPG outputs from Jenkins CI pipelines to provide centralized reporting, historical trends, and implementation metrics for 50+ engineers across multiple ASIC projects
- Built Python-based automation and a JS/HTML dashboard to improve DFT visibility and accelerate regression analysis; recognized by engineering leadership for broader adoption as a standardized reporting solution
- Develop and maintain DFT implementation environments, including filelists, functional timing constraints, and configuration files for Synopsys Testmax, Design Compiler, and ATPG flows
- Collaborate with Logic, Physical Design, and DevOps teams to define project-wide DFT implementation strategy, including macro sequencing, insertion methodologies, chip-level integration planning, and resolution of RTL, elaboration, and synthesis issues

Intel Corporation **Hillsboro, OR**
RTL Design Intern – PLL Team *May 2024 – August 2024*

- Designed and implemented a SystemVerilog RTL bridge between the JTAG Test Access Port (TAP) and PLL configuration registers, replacing generated Tessent bridge logic with an internally developed solution to support migration to the Synopsys DFT flow for next-generation CPU designs
- Developed a comprehensive SystemVerilog testbench which leveraged assertions and Linux shell scripts for simulation and verification via Vivado and Verdi tools such as linting, CDC analysis, and static design checks
- Rebuilt critical IP tools in Python to replace outdated Perl scripts used in parsing my team's RDL metadata into user-friendly CSVs to improve clarity of deliverables to other Intel IP teams, greatly expediting design processes
- Delivered a fully validated and documented RTL IP solution that accelerated internal testing cycles, reduced validation runtime and enabled adoption of Synopsys DFT tools across multiple product lines

L3Harris Technologies **Palm Bay, FL**
Electrical Digital Design Engineering Intern *May 2023 – August 2023*

- Conducted comprehensive FPGA timing verification for a wideband processing card's SPI communication between the primary FPGA and peripheral devices to ensure reliable satellite communication after launch
- Completed FPGA verification training specializing in testbench creation and clock domain crossing techniques
- Simulated and optimized multilayer PCB signal integrity, mitigating reflection and overshoot

Element Solutions | MacDermid Alpha Electronics Solutions **Johns Creek, GA**
Electrical Engineering Intern *May 2022 – August 2022*

- Updated and enhanced technical datasheets through ASTM and MIL-STD quality control experiments on semiconductor and circuit card manufacturing materials to drive greater customer confidence and product sales
- Identified potential performance improvements that informed next-generation R&D product initiatives